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(54) A method for manufacturing a component and a component produced by the method

(57) A method for manufacturing a component includes etching a layer using three differently-shaped masks through successive intervals of depth, weighted in accordance with a binary sequence (1:2:4). The component produced by the method has 7 discrete steps (i.e. 2^n-1 steps where n is the number of etch stages). The method can be used to produce a stepped edge region (bounding a contact hole) in the field oxide layer of a MOS field effect transistor. A metallisation layer is deposited on the stepped edge region with improved coverage.

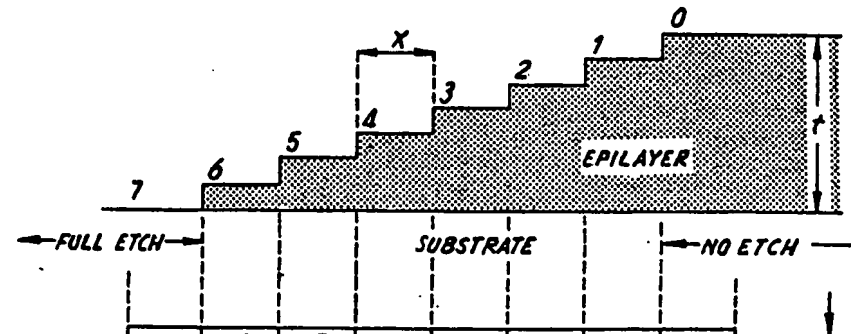

FIG.4

ZONE	7	6	5	4	3	2	1	0	ETCH DEPTH	STAGE
	1	0	1	0	1	0	1	0	t/7 ETCH	I
	1	1	0	0	1	1	0	0	2t/7 ETCH	II
	1	1	1	1	0	0	0	0	4t/7 ETCH	III

KEY : 1=ETCH (CLEAR) ; 0 = NO ETCH (DARK)

TABLE 1

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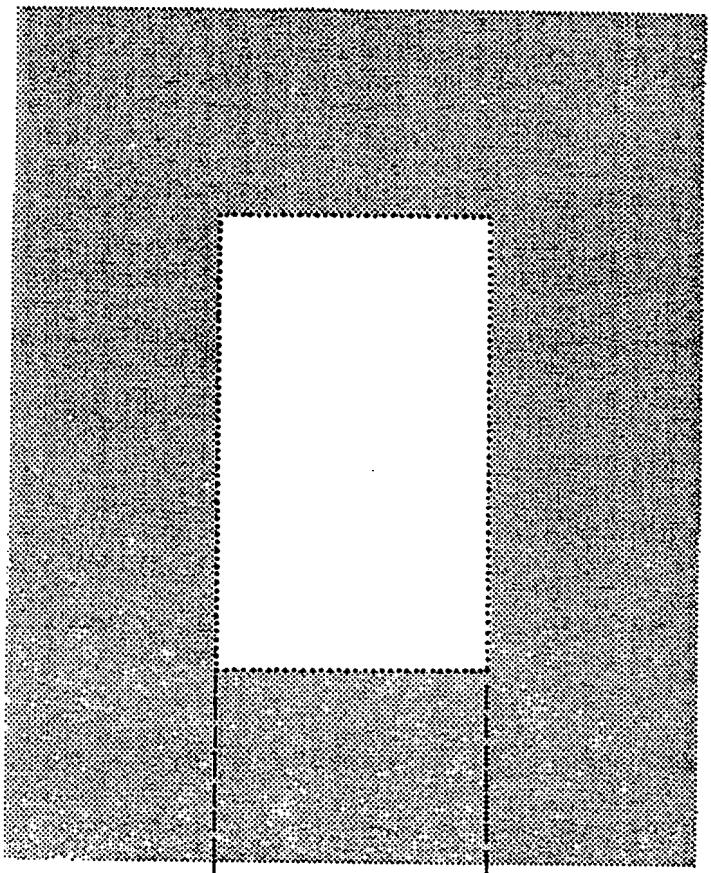
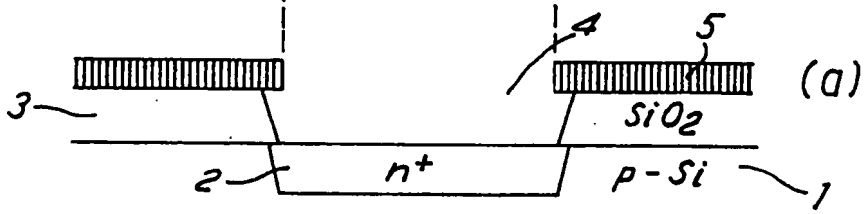
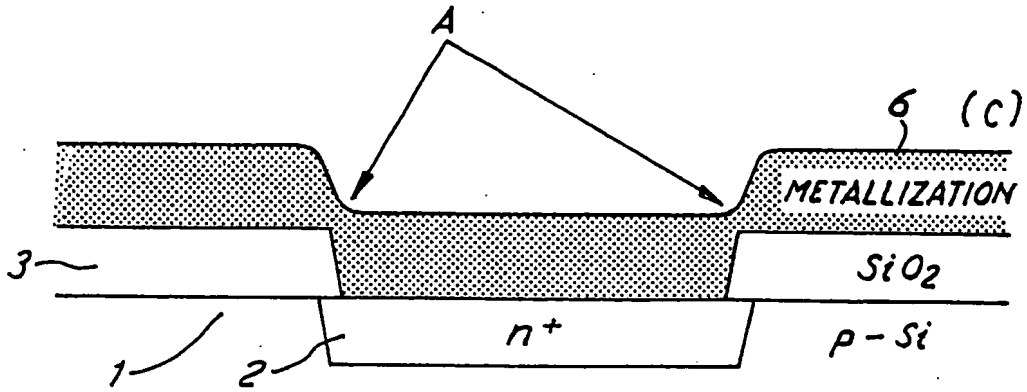


FIG.1

(b)





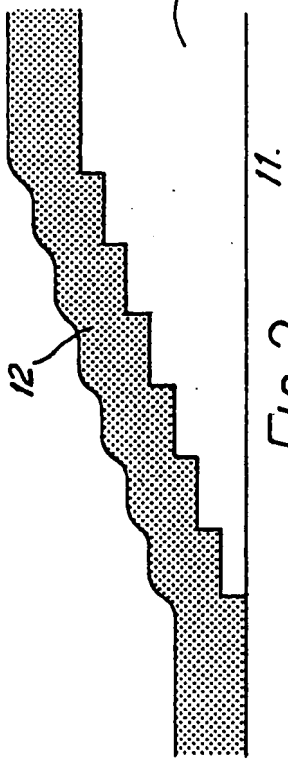
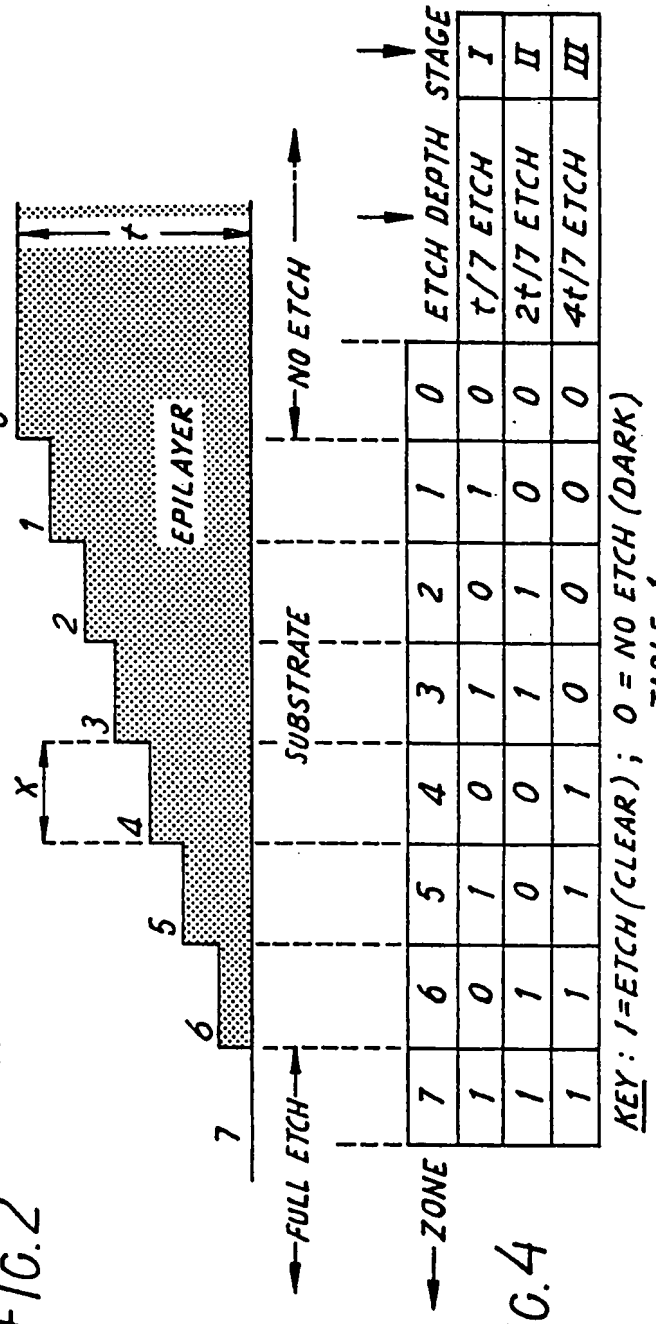


FIG. 2



7	6	5	4	3	2	1	0	ETCH DEPTH	STAGE
1	0	1	0	1	0	1	0	t/7 ETCH	I
1	1	0	0	1	1	0	0	2t/7 ETCH	II
1	1	1	1	0	0	0	0	4t/7 ETCH	III

KEY : 1=ETCH (CLEAR) ; 0 = NO ETCH (DARK)

TABLE 1

FIG. 4

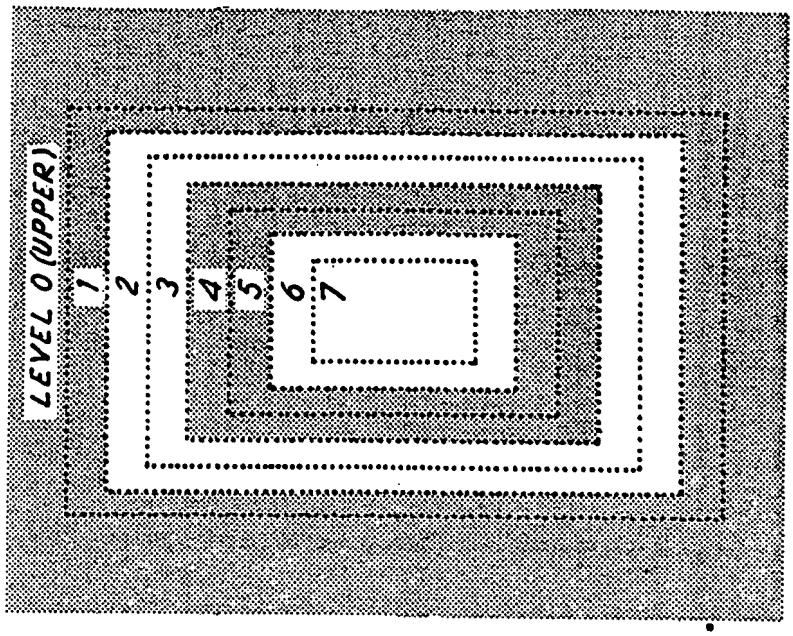


FIG.3(b)

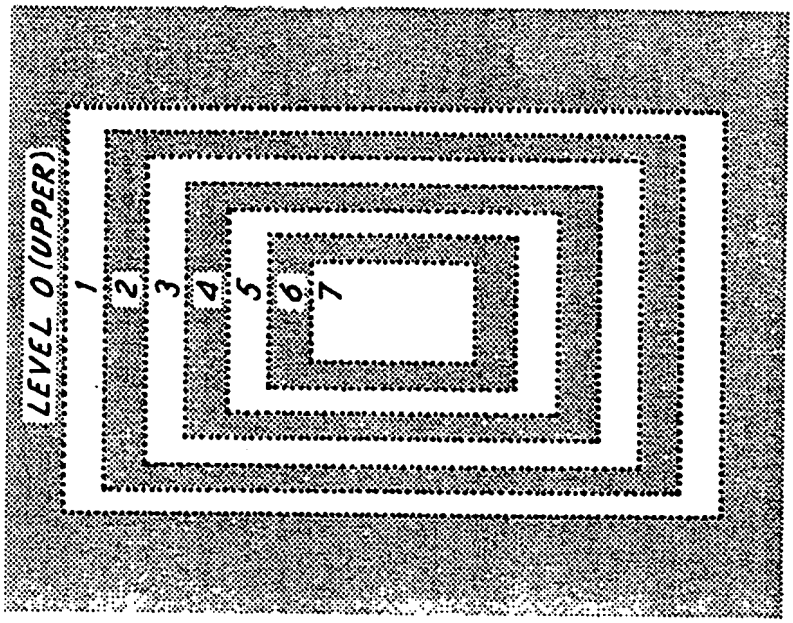


FIG.3(a)

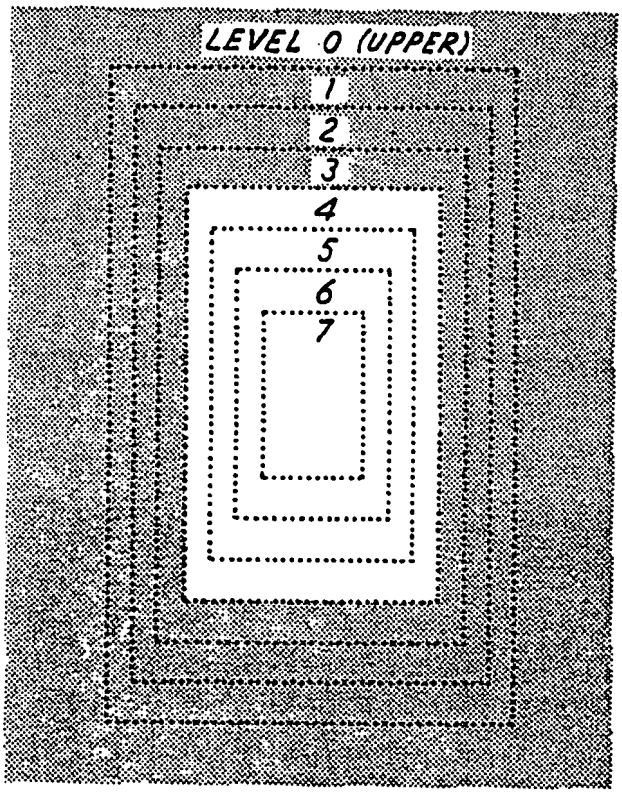


FIG. 3(c)

SPECIFICATION

A method of manufacturing a component and a component produced by the method

This invention relates to a method for manufacturing a component and it relates particularly, though not exclusively, to a method for manufacturing a semiconductor component (e.g. an electrical device such as a MOS field effect transistor) using so-called planar fabrication techniques. The invention also relates to a component produced by the method.

Many electrical devices are manufactured using so-called planar fabrication techniques whereby individual elements of a device are formed in a single plane typically at a surface of a single crystal of silicon. Since, in general, several processing stages may be needed to fabricate the device the surface topology of the crystal is found, in practice, to be far from planar and may contain steep edges, some as deep as 2μm.

These edges can be troublesome if a thin, continuous film is to be deposited at the crystal surface, especially if the film thickness is less than, or similar to, the depth of an edge.

A problem may be encountered, for example, in forming an electrical contact with the drain, source or semiconductor bulk regions of a metal-oxide-semiconductor field effect transistor (MOSFET).

The problem is illustrated by reference to Figure 1a of the accompanying drawings which represents one stage in the formation of an electrical contact. The figure shows a cross-sectional view through a substrate 1 of p-type silicon formed with a n^+-type diffusion region 2 constituting the drain (or source) region of the device. A field oxide layer 3 of silicon dioxide overlies the substrate and is provided with a contact hole 4 exposing the diffusion region.

The contact hole is formed by means of a photolithographic technique whereby a selected region of a layer 5 of a photoresist material is exposed to ultraviolet radiation through a suitably configured shadow mask thereby to permit etching of a desired region of the oxide layer. In this, and subsequently described, examples a positive photoresist, such as that known as Shipley AZ1350, is used, those regions which are exposed to radiation being susceptible to developing and etching. Figure 1b represents a plan view of the shadow mask used in this example, the shaded part of the mask being non-transmissive of radiation and so preventing etching and the clear part being transmissive and permitting etching. Once etching is complete and hole 4 has been formed, any residual photoresist is removed and a metal film, shown at 6 in Figure 1c of the drawings, is deposited (typically by thermal evaporation in a vacuum or by sputtering), thereby to establish an electrical contact with diffusion region 2. Typically the film is about 1μm thick though, as will be apparent from Figure 1c, the film has relatively thin regions, designated "A" in the drawing, where the metal covers an edge region, typically 0.5-1μm deep, formed by the sides of hole 4. These sparsely covered regions are particularly prone to cracking due to thermal stress thus tending to cause an electrical discontinuity. Moreover, because the local resistivity of the film tends to be high in these regions the film is susceptible to burn-out and electromigration. These problems tend to degrade overall performance and reliability of the device and to limit its operational lifetime.

A similar problem may be encountered in forming an electrical contact with the gate region of a MOSFET. The gate oxide layer is typically 0.1 μm thick whereas the field oxide layer, which borders the gate oxide layer, is typically 1 μm thick. Consequently a metallisation film for establishing an electrical contact must cover a relatively steep edge, typically about 1 μm deep. In some forms of MOSFET, for example, where the device has been modified to be a gas-sensitive field-effect transistor (GASFET) a very thin gate electrode, typically 10 nm thick, of a catalytically active metal such as palladium or platinum is used and in these circumstances the electrode must cover two different edges, firstly due to the field oxide layer, and secondly due to a metal track which is typically 1 μm thick and connects the electrode to a bonding pad.

Edge coverage problems may be encountered also in other contexts. For example, some devices such as microwave devices, power transistors and power rectifiers are fabricated so as to be intrinsically non-planar. Also in some VLSI applications complex interconnections are required wherein two or more metallisation layers are arranged in stacked relationship with thin insulating films of SiO_2 or polyimide separating adjacent layers. With this kind of construction a metallisation layer may cross one or more edges created by an underlying metallisation and or insulation layer.

It will be apparent from the aforementioned examples that edge coverage problems abound in the fabrication of many electrical devices. Attempts have been made to improve step coverage and in one known technique, described by Y.I. Choi et al in IEE Proc, Vol 133, Pt I, No.1 February 1986, a hole formed in a layer of thermally grown silicon dioxide was tapered controllably by selective heat treatment of a thin layer of silicafilm applied to the oxide layer prior to etching. While it is possible to achieve improved coverage of the sides of the hole, the technique has not, in general, proved to be sufficiently reproducible and reliable for many practical applications.

It is one object of the present invention to provide an improved fabrication technique whereby the above-described problems may at

least be alleviated.

According to a first aspect of the invention there is provided a method for manufacturing a component, the method including etching a layer of a material in accordance with each of a number of differently shaped patterns thereby to produce an edge region consisting of a series of discrete step formations arranged at successive levels in the layer.

The method may include etching said layer in accordance with n differently shaped patterns through successive intervals of depth weighted in accordance with a binary sequence, whereby said edge region consists of 2^n-1 of said discrete steps and may further include depositing a further layer on said edge region.

According to another aspect of the invention there is provided a component produced by a method according to said first aspect of the invention. The component produced by said method may be in the form of a metal-oxide-semiconductor field effect transistor wherein said layer of a material comprises a field oxide layer, said edge region bounds a contact region formed in the field oxide layer and said further layer comprises a metallisation for establishing an electrical contact with a surface exposed by said contact region. Said contact region may be a contact hole which exposes a drain, source or semiconductor bulk region of the device or a gate insulation region of the device.

According to a yet further aspect of the invention there is provided a component in the form of an electrical device including a layer of a first material having an edge region, and a layer of a second material overlying said edge region, wherein said edge region comprises a series of discrete, step formations arranged at successive levels in said layer of a first material.

The inventor has found that a stepped configuration of the kind defined is remarkably effective in promoting coverage of said edge region by said second material.

In order that the invention may be carried readily into effect an embodiment thereof is now described, by way of example only, by reference to Figures 2 to 4 of the accompanying drawings of which,

Figure 1a shows a cross-sectional view through part of a MOSFET to illustrate processing of a contact hole,

Figure 1b shows a plan view of a shadow mask used to process the contact hole of Figure 1a,

Figure 1c shows a cross-sectional view through the contact hole with a metallisation layer applied,

Figure 2 shows a cross-sectional view through a stepped edge region in accordance with the present invention,

Figures 3a, 3b and 3c shows respective plan views of different shadow masks used in a fabrication technique in accordance with the invention and

Figure 4 shows a cross-sectional view through an edge region to illustrate the fabrication technique.

Figure 2 of the drawings shows a detailed cross-sectional view through an edge region of an epitaxial layer 10 formed on a substrate 11. In one example of the invention layer 10 might comprise the field oxide layer of a MOSFET with the edge region bounding a contact hole, and a layer 12 overlying the edge region could then comprise a metallisation film effective to establish an electrical contact with the drain, source or bulk semiconductor regions of the device at an exposed surface of the substrate. It will be appreciated, however, that in other applications of this invention either layer 10 or layer 12 could comprise a metal, a semi-conductor or an insulator such as an oxide or an organic material.

As shown in Figure 2, the edge region is formed as a series of discrete steps which are arranged at successive levels in the epitaxial layer, rather in the manner of a staircase, and the inventor finds that this configuration leads to improved coverage of the edge region. It will be apparent that in contrast to prior configurations, as illustrated in Figure 1c for example, layer 12 is signficantly thinner than layer 10 on which it is deposited and yet is relatively free from the irregularities and relatively thin regions (A in Figure 1c) which have proved to be so troublesome hitherto. Thus if layer 12 comprises a metallisation, a configuration in accordance with the present invention should be less susceptible to electrical discontinuity, burn-out and electromigration.

The inventor has discovered that a stepped edge region of the kind described may be fabricated in a relatively straight forward manner by means of a multi-stage etch process whereby a different, appropriately configured shadow mask is used at each successive stage in the process and successive etch depths, controlled by the duration of each etch, are weighted in accordance with a binary sequence (i.e. in the ratio 1:2:4: etc). By use of appropriately configured shadow masks the inventor finds that the total etch depth attained at any particular location in the edge region is equal to the sum of the individual etch depths to which that location has been subjected, thus producing a total of 2^n different levels or 2^n-1 different steps, where n equals the number of etch stages used. Thus, whereas a known, single stage etch process ($n=1$) yields 2 levels (i.e. 1 step -Figure 1a), a dual stage process ($n=2$) yields 4 levels (i.e. 3 steps) and a triple stage process ($n=3$) yields 8 levels (i.e. 7 steps) and so on.

The etch process will now be described in greater detail by reference to the triple stage process ($n=3$), and Figures 3a, 3b and 3c

show plan views of the shadow masks used during the first, second and third stages respectively of the process thereby to produce a rectangular contact hole in the field oxide layer of a MOSFET.

For clarity of illustration, Figure 4 represents a cross-sectional view through one side only of the contact hole and different zones, defining the positions of different levels in the edge region, are designated in Figures 3 and 4 by numbers 0 to 7.

The uppermost level (zone 0), at the surface of the epitaxial layer, requires no etching and this is represented as an entry "0" (no etch) in a corresponding column of Table I, accompanying Figure 4, at each of the three stages I, II, III of the etch process, and as a dark region in each shadow mask.

In contrast, the lowermost level (zone 7) requires full etching, represented as an entry "1" (etch) in the table at each stage in the process, and as a clear area in each mask. In this example, the seven steps produced by the etch process are of equal depth t/7, where t is the thickness of the epitaxial layer, and the length x of each step may be as small as the process minimum feature size will allow, typically several microns. As described hereinbefore, successive etch depths are weighted in accordance with a binary sequence (i.e in the ratio 1:2:4). The step height t/7 defines the minimum etch depth required, and this is applied in the first stage (I) of the etch process, and the etch depths for the second (II) and third (III) stages in the process take the values 2/7t and 4/7t respectively. The etch period corresponding to each etch depth is determined by timing complete removal of the epitaxial layer from a test wafer and calculating the appropriate proportion of the measured period.

It will be appreciated that the dark and clear areas of each shadow mask are so arranged as to mask zones 0 to 7 of the epitaxial layer in accordance with the scheme set out in Table 1 thereby to generate a stepped edge region as shown in Figures 2 and 4. Thus, for example, zone 6 of the epitaxial layer is subjected to etching during the second and third stages only of the process. The etch depths which apply in the second and third stages are 2/7t and 4/7t respectively and so the total etch depth attained is 6/7t, so that the level produced in zone 6 occurs at a depth 6/7ths of the way through the epitaxial layer.

It will be understood that although the above-described method is applicable to the fabrication of an electrical device such as a MOS devices, for example a MOSFET-based chemical sensors, including GasFET devices, the present invention is considered to be applicable generally to the fabrication of discrete components including circuits. The invention is likely to find application in the field of silicon micromachining, for the production of components having specific topologies, for example tapered or wedge-shaped films and components having precisely defined features such as grooves, pits and depressions. Substantially pyramidal, domed or hemi cylindrical components produced by the method of this invention could find application in integrated optics, such as a micro lens or waveguide, for example. The invention is also applicable to Langumuir-Blodgett device technology.

CLAIMS

1. A method for manufacturing a component, the method including etching a layer of a material in accordance with each of a number of differently shaped patterns thereby to produce an edge region consisting of a series of discrete step formations arranged at successive levels in the layer.

2. A method according to Claim 2 including etching said layer in accordance with n differently shaped patterns through successive intervals of depth weighted in accordance with a binary sequence, whereby said edge region consists of 2^n-1 of said discrete steps.

3. A method according to Claim 1 or Claim 2 including depositing a further layer on said edge region.

4. A component produced by a method according to any one of Claims 1 to 3.

5. A component according to Claim 4 in the form of a metal-oxide-semiconductor field effect transistor wherein said layer of a material comprises a field oxide layer, said edge region bounds a contact region formed in the field oxide layer and said further layer comprises a metallisation for establishing an electrical contact with a surface exposed by said contact region.

6. A component according to Claim 5 wherein said contact region is a contact hole which exposes a drain, source or semiconductor bulk region of the device.

7. A component according to Claim 5 wherein said contact region exposes a gate insulation layer of the device.

8. A component in the form of an electrical device including a layer of a first material having an edge region, and a layer of a second material overlying said edge region, wherein said edge region comprises a series of discrete, step formations arranged at successive levels in said layer of a first material.

9. A method for manufacturing a component substantially as hereinbefore described by reference to Figures 2 to 4 of the accompanying drawings.

10. A component substantially as hereinbefore described by reference to Figures 2 to 4 of the accompanying drawings.

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